

ABSTRACT OF THE DISCLOSURE

A self-test controller 10 for memory devices 6, 8 is provided with an integrated circuit

2. The self-test controller 10 produces physical memory address values Xaddr, Yaddr for
5 driving desired memory tests. A mapping circuit 24, 26 serves to map these physical
memory address signals to logical memory address signals LA[8:0] as required by the
particular memory devices 6, 8. In this way a generic self-test controller may be provided
that is able to drive tests within multiple different memory devices 6, 8 by providing a
relatively simple mapping circuit 24, 26.

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[Figure 5]